Claims

[c1] 1. A method of causing a test equipment to accurately place the edges of a signal used to test a device under test (DUT), said method being performed in a digital processing system, said method comprising:
determining an expected time of occurrence of each edge of said signal;
instructing said test equipment to generate a plurality of cycles of said signal in relation to said tester cycle time;
receiving data indicating a plurality of time points at which the edges of said signal have occurred in said plurality of cycles;
computing an error based on said plurality of time points and said expected time; and
adjusting a timing of the edges of said signal based on said error.

[c2] 2. The method of claim 1, wherein each of said expected time and said plurality of time points are indicated in relation to a tester cycle time of said test equipment.

[c3] 3. The method of claim 2, wherein said plurality of time points comprise at least ten time points.

[c4] 4. The method of claim 2, further comprising sending a command to configure a device under test (DUT) interface board to loop back said signal to said test equipment.

[c5] 5. The method of claim 4, further comprising performing the elements of claim 1 until said error is within an acceptable range.

[c6] 6. The method of claim 2, wherein said computing comprises:
determining a mean value of said plurality of time points; and
setting said error to equal a difference of said mean value and said expected time.

[c7] 7. The method of claim 6, wherein the edges of a clock signal are placed accurately by using said clock signal as said signal, and the edges of a data signal are placed accurately by using said data signal as said signal such that said data signal can be sampled accurately using said clock signal in said DUT.

[c8] 8. The method of claim 7, further comprising sending to said test equipment a threshold voltage level, said threshold voltage level indicating a voltage level at which said signal is deemed to have transitioned from one logic

level to another, wherein said test equipment compares said threshold voltage level to a voltage level of said signal a plurality of times in each tester cycle and provides a comparison result, wherein said data comprises said comparison result and a time of comparison.

[c9] 9. A machine readable medium carrying one or more sequences of instructions for causing a digital processing system to control a test equipment to accurately place the edges of a signal used to test a device under test (DUT), wherein execution of said one or more sequences of instructions by one or more processors contained in said digital processing system causes said one or more processors to perform the actions of:
determining an expected time of occurrence of each edge of said signal;
instructing said test equipment to generate a plurality of cycles of said signal in relation to said tester cycle time;
receiving data indicating a plurality of time points at which the edges of said signal have occurred in said plurality of cycles;
computing an error based on said plurality of time points and said expected time; and
adjusting a timing of the edges of said signal based on said error.

[c10] 10. The machine readable medium of claim 9, wherein each of said expected time and said plurality of time points are indicated in relation to a tester cycle time of said test equipment.

[c11] 11. The machine readable medium of claim 10, wherein said plurality of time points comprise at least ten time points.

[c12] 12. The machine readable medium of claim 10, further comprising sending a command to configure a device under test (DUT) interface board to loop back said signal to said test equipment.

[c13] 13. The machine readable medium of claim 12, further comprising performing the elements of claim 11 until said error is within an acceptable range.

[c14] 14. The machine readable medium of claim 10, wherein said computing comprises:
determining a mean value of said plurality of time points; and
setting said error to equal a difference of said mean value and said expected time.

[c15] 15. The machine readable medium of claim 14, wherein the edges of a clock signal are placed accurately by using said clock signal as said signal, and the edges of a

data signal are placed accurately by using said data signal as said signal such that said data signal can be sampled accurately using said clock signal in said DUT.

[c16] 16. The machine readable medium of claim 15, further comprising sending to said test equipment a threshold voltage level, said threshold voltage level indicating a voltage level at which said signal is deemed to have transitioned from one logic level to another, wherein said test equipment compares said threshold voltage level to a voltage level of said signal a plurality of times in each tester cycle and provides a comparison result, wherein said data comprises said comparison result and a time of comparison.